**EE 465 Lab Report**

*Lab 6 – Placement and Routing*

Written by: Anh Q. Ho, Aaron Pederson

Lab Section – Monday 04:10pm

Abstract

Synthesis procedures are truly depends on how the architecture or system engineers set their constraints since they design and know when and what signals should go where. By setting constraints, students can emulate the real working environment for the design of this experiment. In this lab, students are to only cover the most important and common used constraints in the semiconductor industries.

Introduction

In this lab, students are to run placement and routing for the synthesized net-lists of Lab 4 using Cadence Encounter.

Objectives

* Placement and Routing
* Circuit timing, area, power analysis after placement and routing

Students are to follow the design flow below to achieve their goal.

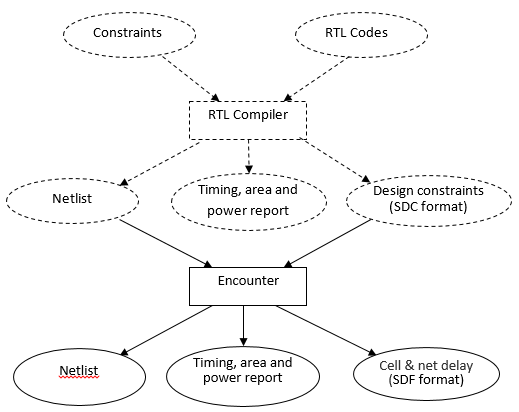


Figure - Lab 6 design flow.

In order to have a success in this lab; there are multiple tasks that are required for this lab:

1. Go through the attached placement and routing document at the end of this report
2. Based on timing, area, and power report, fine tune the parameters in placement and routing flow to optimize the design. The goals are:
   1. Small clock period while no timing violation for both setup time and hold time.
      1. The following setup is to check for timing violation
         * Select Hold at “Optimize” →“Optimize Design” step.
   2. Small area
   3. Less Power Consumption
3. Report the best clock period, area and power consumption that the group can achieve.

Please refer to the attached document encounter-instructions.docx regarding how to use Cadence Encounter to do placement and routing.

results & Discussion

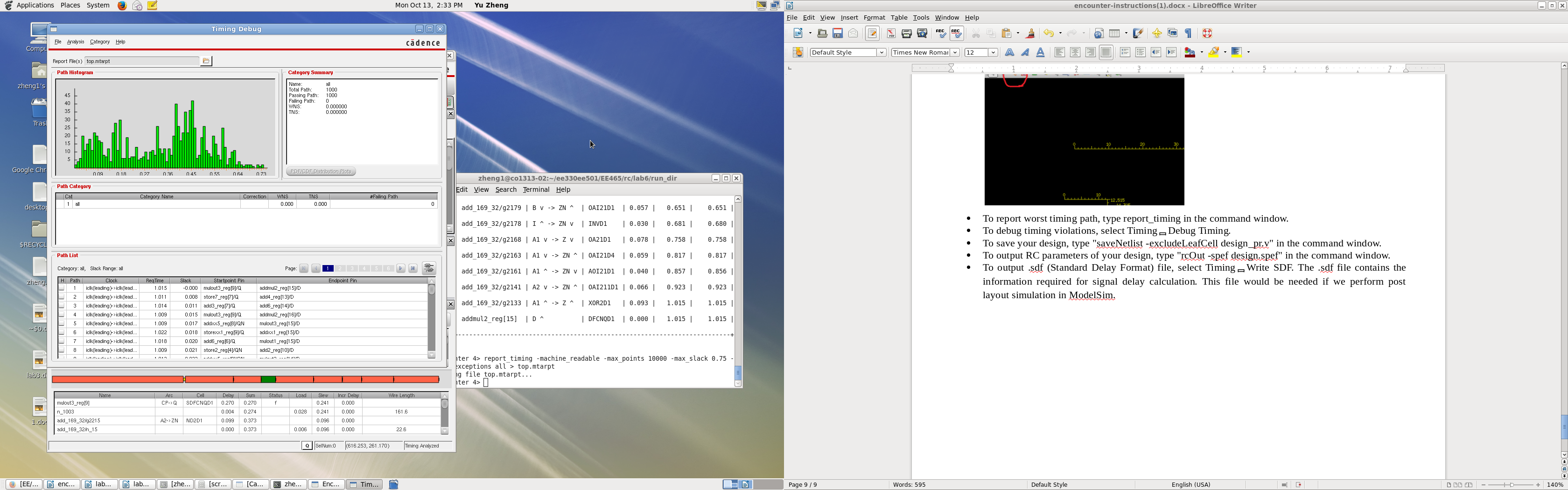


Figure - Timing report of the optimized chip

As in the graph in figure 2 shows that there are 1000 paths in the chip but the slowest time of all paths is approximately 0.45µs.

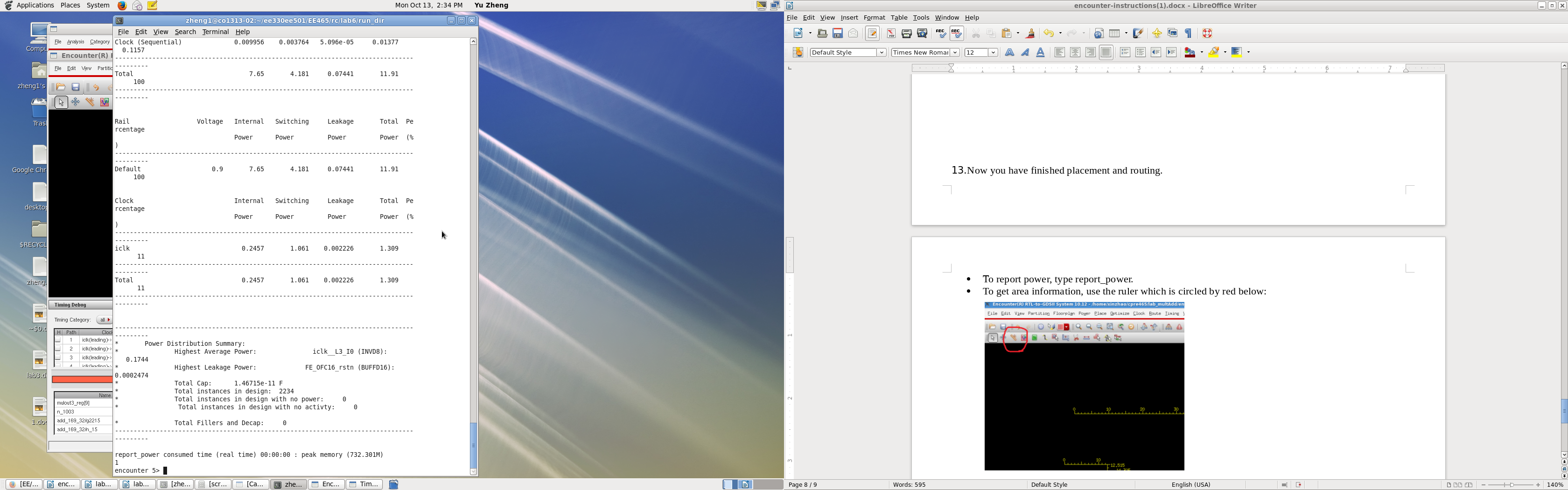


Figure - Total Power consumption report

The total power consumption of the optimized chip is around 11.91mW with the internal power of 7.65 switching power of 4.18 and the leakage of around 0.074mW lost.

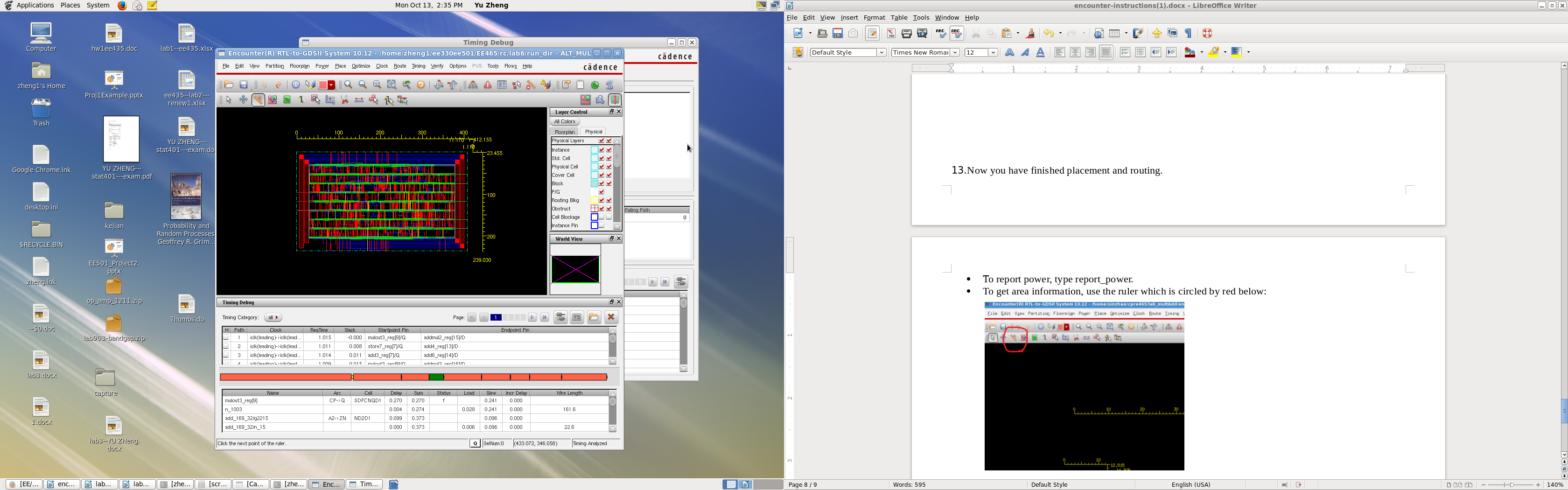


Figure 4 - Capture of the optimized Chip with the least area.

The area in figure 2 is approximately .

Conclusion

The lab went fairly well for the group, the only concerns were the commands as mentioned before working on this lab (NOTE), the groups were using quite a bit of time trying to determine the problem since the lab manual instructed to save the file as “ALT\_MULTADD” but not saying much about the naming of the module. Otherwise, the minor issues is how much to change on the timing constraints. At first, all changes were half of the original values, but not much were changed in the reports. Thus a change in a factor of ten, the alteration were well spotted.